Multi-Channel Transcutaneous Cortical Stimulation System

Contract # N01-NS-7-2365

Progress Report #16

for the contract period 2/1/01 – 4/30/01

Illinois Institute of Technology

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The goal of this project is the design, fabrication, and testing of a ***Multi-Channel Transcutaneous Cortical Stimulation System*** to be used in a prototype artificial vision system**.** During the past 25 years, the development of a neuroprosthesis that could be used to restore visual sensory functions has been an important goal of the Neural Prosthesis Program (NPP) of the National Institute of Disorders and Stroke, National Institutes of Health. Demonstrations of the feasibility of a visual prosthesis have reached the stage in which the NPP is highly motivated to initiate the development of a fully implantable cortical stimulation system which could be used to provide inputs and computer control for hundreds, to over one thousand, implanted cortical electrodes. This is the sixteenth progress report for this project. In this report we describe testing of the 8-channel BLOCK chip design that uses extended drain transistors to compensate for residual error current seen for large voltages across the biphasic electrode drivers.

Figure 1, below shows the schematic of the BLOCK chip output stage.

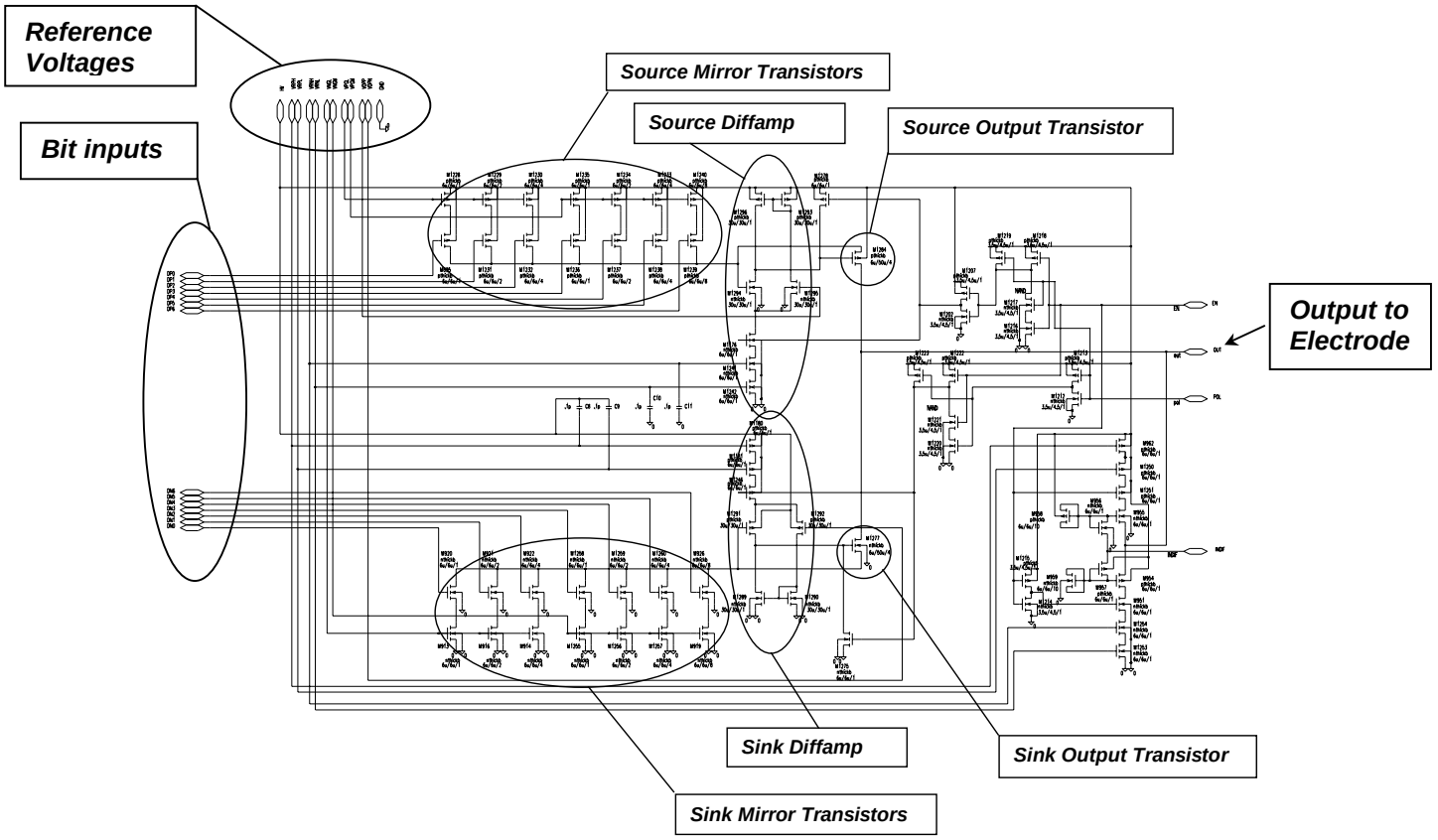


Figure 1 – Schematic of the BLOCK chip output stage showing major functional elements

The basic operation of this circuit is as follows: The biphasic waveform is controlled by two sets of current mirrors. One for the anodic (Source) current, and one for the cathodic (Sink) current. There are seven current mirrors for the both the Source and Sink currents. Each mirror represents a bit of the seven-bit amplitude-controlled biphasic current driver. The transistors are sized, as parallel multiple transistors, to provide the appropriate weighting for each of the bits. The gate bias voltages for the seven current mirrors are provided, from the bias reference generator, in two groups: 3 lower order bits, and 4 higher order bits. This division is used, rather than using

one bias voltage for all of the bits, so that the total number of transistors may be reduced. If we used only one bias voltage for all seven bits, then the highest order bit would require 64 transistors in parallel, and the total number of transistors needed for the entire driver would be 127 for the Source and Sink stages, for a total of 254 transistors. In the scheme shown in Figure 1, the 4 higher order bits are supplied with a gate bias such that a unit transistor will be controlled to supply current that is 8 times that of the unit transistor of the 3 lower order bits. Therefore only 22 transistors for all seven Source (or Sink) drivers are needed, for a total of 44, rather than 254, total transistors. The consequence of using this topology is that there needs to be precise control of the two bias voltages supplying the lower and the higher order bits. This is accomplished in a complex and specialized reference generator circuit.

In series with each current mirror is a switch that is controlled by the bit inputs to the circuit. All of the current mirrors, for the Source and Sink drivers, respectively, have their drains connected to a common point. This common point is connected to the source of the respective Source and Sink output transistors. The voltage at these common nodes is controlled by a feedback amplifier, that matches the drain voltage of the all of the current mirrors to that in the bias reference generator circuit. This is accomplished by controlling the gate voltages on the output transistors. In this manner, the combination of the current mirrors and the output transistors form a cascode circuit. Using a cascode corrects for the non-flat characteristic curves of the output transistors. The common node is regulated to a voltage that is approximately 0.5 volts away from the respective power supplies. This provides an extremely wide compliance voltage range with almost flat Source and Sink current curves, with varying electrode voltage.

In spite of the success of these circuit topologies we were left with some residual non-balance between the anodic and cathodic phases of the biphasic current waveform. This imbalance can be seen in the plot of Figure 2, below.

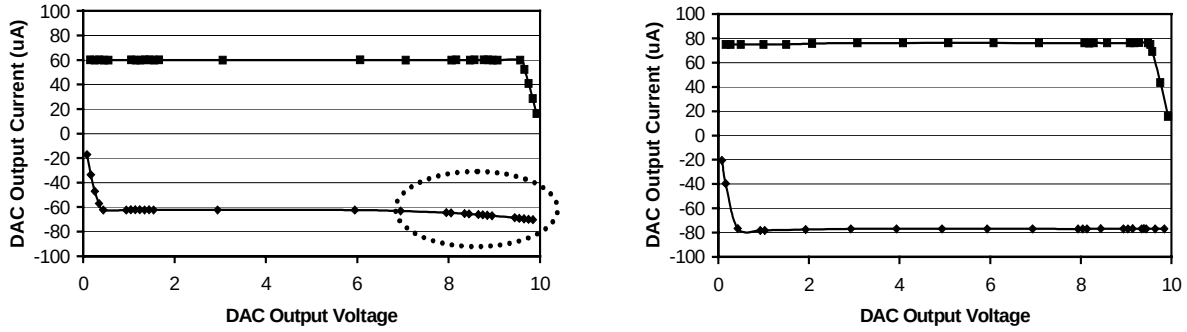


Figure 2 – Left: Residual imbalance in biphasic current. Right: New topology corrects the imbalance.

The residual current, for the Sink drivers was caused by impact ionization current that the cascode circuit was unable to correct. It must be that this current is substrate current, otherwise the cascode circuit would have corrected it. In Figure 3, below, a diagram of an ideal FET and channel are shown. Note that the channel profile linearly changes from the source to the drain of the transistor.

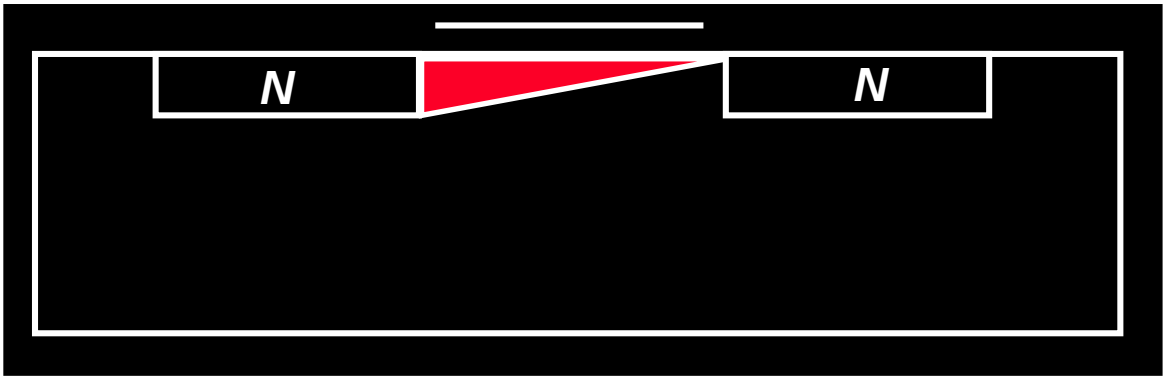


Figure 3 – Ideal channel profile for an FET.

In Figure 4, below, the impact ionization effect is shown. Increased voltage on the drain (shown on the right N region), causes shortening of the channel due to a depletion region around the drain. As the carriers leave the channel they complete the path to the drain by means of drift mechanism. As the channel shortens, the velocity of the carriers increases. As they leave the channel, the carriers impact into the crystal lattice and cause the creation of pairs within the substrate. This current becomes base current for the lateral NPN bipolar transistor. It is this current that results in the impact ionization current.

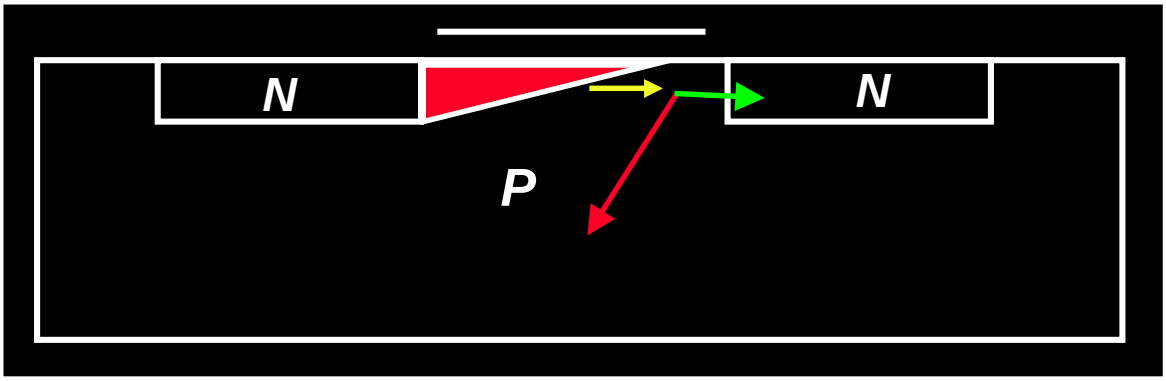


Figure 4 – Diagram showing impact ionization current effect.

The consequence of this current are the non-ideal characteristic curves shown in Figure 5 below.

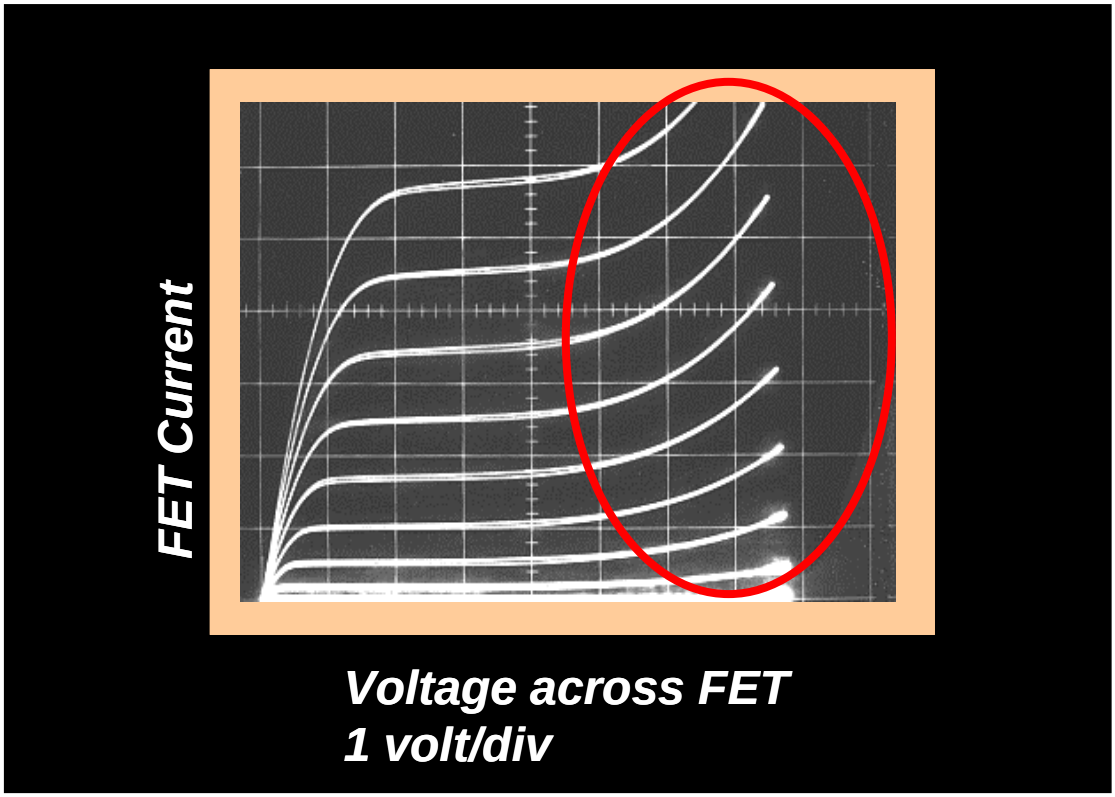


Figure 5 – Non-ideal characteristic curves due to impact ionization. Problematic current is circled in red.

We have implemented an extended drain transistor for the output transistors to correct for the residual imbalance. The extended drain transistor uses a diffusion around the drain to smooth out the electric field in the vicinity of the channel. This dramatically reduces the impact ionization effect. In Figure 2, above, one can see the improved performance in the right-hand plot.

We have now completed testing of this version of the BLOCK chip. We have ordered a larger number of these chips and plan to use them in a design of a 128 channel benchtop stimulator. This stimulator will allow for the testing of the BLOCK chip design with actual microelectrodes that we will obtain from other NPW researchers.

at and analysis of the Macor ceramic package.

Figure 1 reviews the basic structure of the ceramic multichip module. In this figure can be seen the location of the glass-to-ceramic seal, located on layer#2. Since the module is comprised of 4 layers of ceramic, there are 3 identically configured glass seals in a complete module.

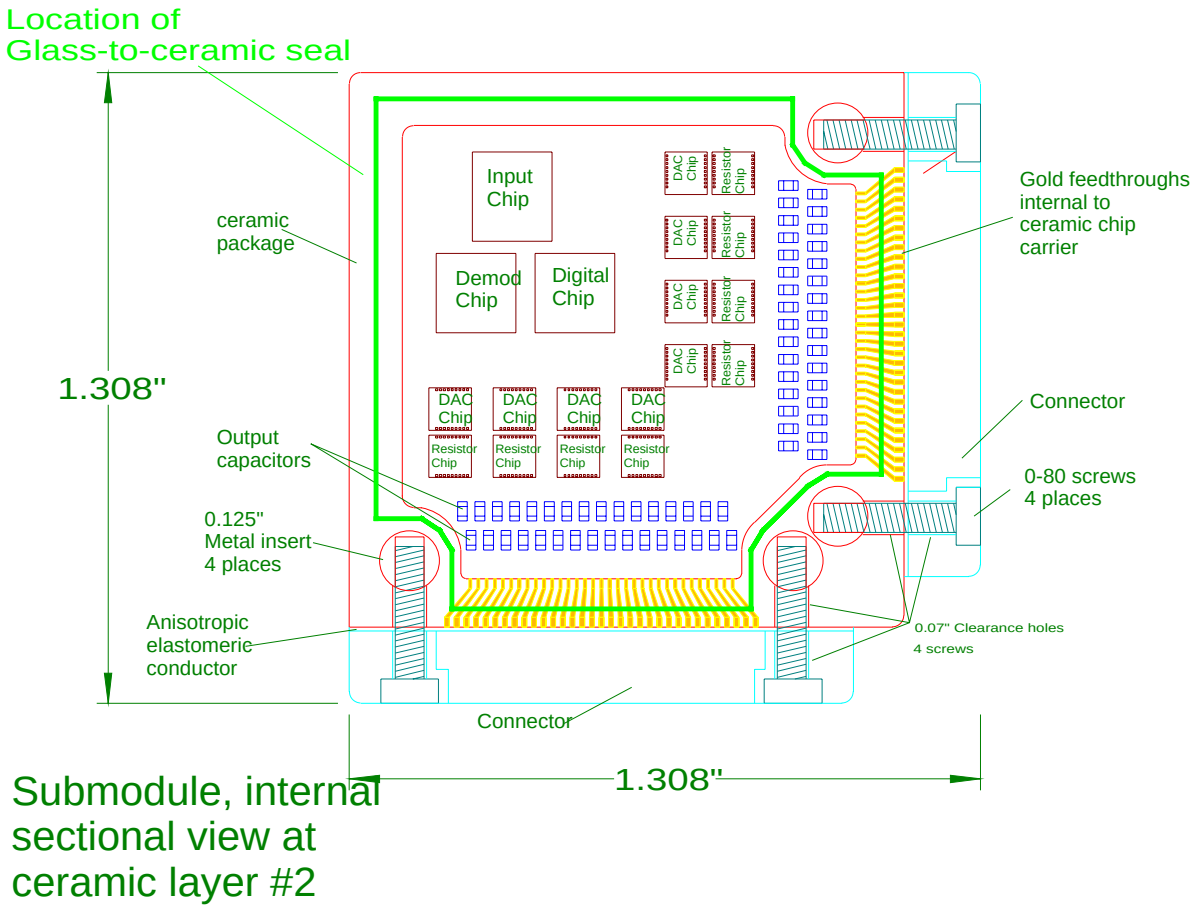
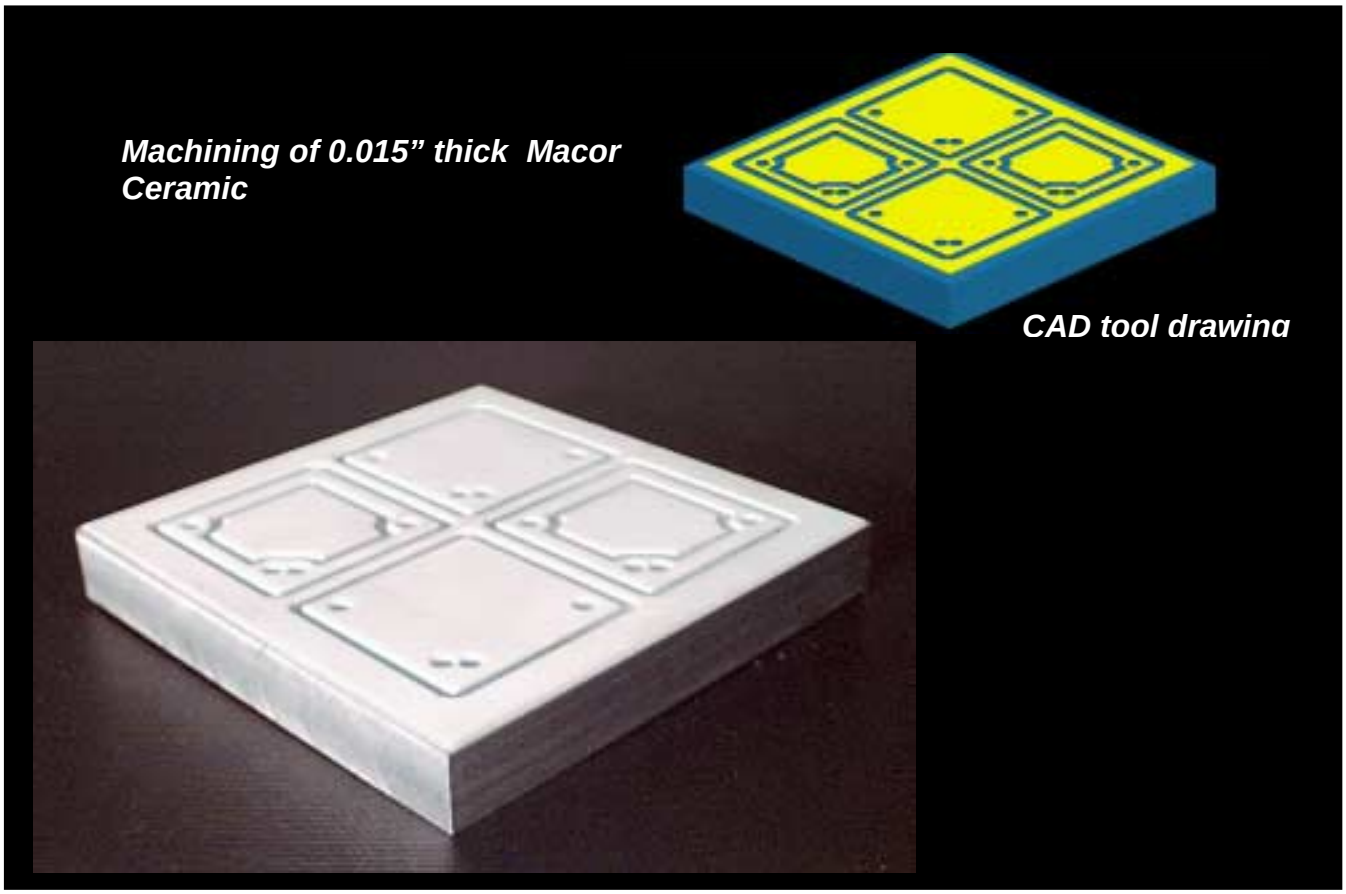


Figure 1 – Sectional drawing of the implant package showing the location of the glass seal.

In order to test the integrity of the glass seal, we fabricated a prototype package comprised of 4 layers of ceramic that were cut in the shape dictated by the package design. These can be seen in Figure 2, below. In the upper right of Figure 2 is shown the CAD tool drawing, from AUTOCAD, that is used as input into the numerically-controlled milling machine.

Figure 2 – Machine tool drawing shown next to fully machined ceramic sheets.

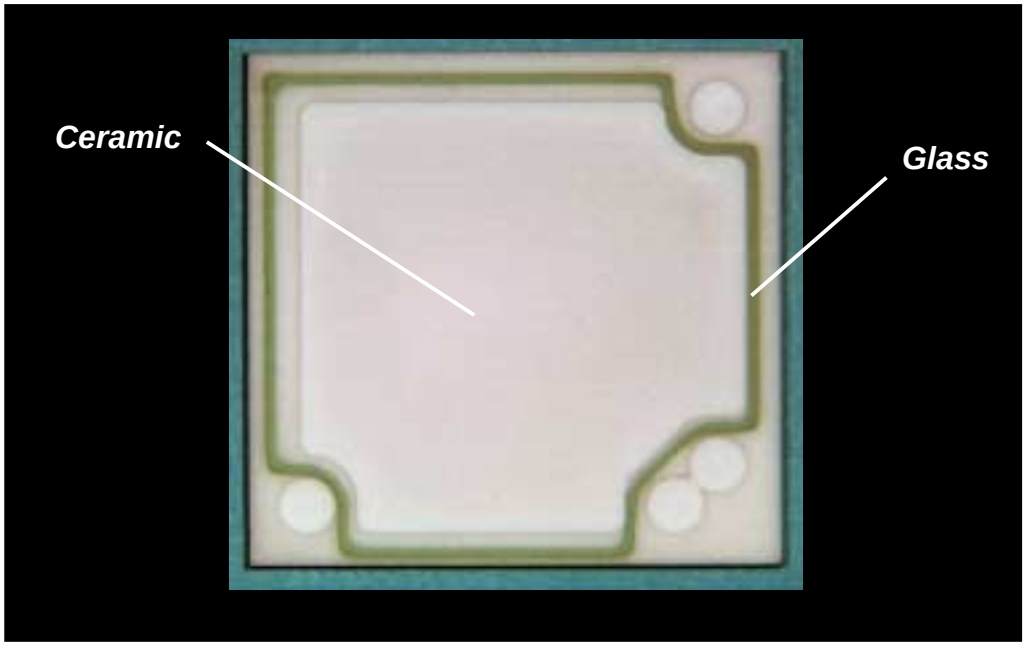
The 0.015” thick ceramic sheet is held down on the lapped tool aluminum block using paraffin. The milling machine automatically cuts the shape of all four layers, for a single package,



in less than 20 minutes. Once the machining operation is completed, the ceramic is removed from the aluminum block by heating on a hot plate. The paraffin is removed from the ceramic by placing the individual cut pieces, for each layer, on the hot plate, between two layers of absorbent material while weighting down with a steel block. This blotting procedure removes almost all of the paraffin. To insure that no residual paraffin remains, the 4 pieces of ceramic are baked in a 450-degree Celsius furnace for several hours.

The glass is deposited in the green state by mixing the power with a deposition vehicle. This slurry is then loaded into a hypodermic syringe. The syringe is placed in a holder attached to a computer-controlled X-Y table. The input to the table controller is an AUTOCAD file that defines the path to be traced by the syringe. The deposition is controlled by an air-powered syringe system, and the activation and deactivation of the syringe flow is synchronized to the computer controlled path of the syringe. A typical piece of ceramic, showing the glass in the green state is shown in Figure 3, below.

Figure 3 – Glass seal deposited on the ceramic while in the green state.



The deposited glass is dried by baking in an oven at 100 degrees Celsius for 24 hours. Then it is prefired at 350 degress Celsius for 2 days. This is necessary to bake off the vehicle prior to firing of the seal. The 4 layers of ceramic, with the green-state seals, are carefully loaded into a stainless steel fixture that uses weight to apply a compressive force to the ceramic layers. The fixture is then placed in the electronically-controlled furnace for the ramped firing profile. The glass is fired at 385 degrees Celsius. The ramped profile includes a dwell time, just below the firing temperature to allow pressure equalization within the package relative to the external environment. This is important to prevent "blow-out" of the seal. A passive, ramped cool-down cycle minimizes the residual stress in the seal.

Package type		
Blank Macor	6×10^{-8}	1×10^{-9}
Sealed	1×10^{-7}	4×10^{-9}

Helium bomb = 45 psi
Background = 10^{-11}

cc-atm/sec

We sent a prototype package to the Mann Foundation for Helium leak testing. In this test, the package is Helium-bombed at 45 PSI. Then the residual Helium emanating from the package is measured. As a control, we used a solid piece of Macor, of approximately the same dimensions as the prototype package. The results from this test are shown in Table 1, above. Note that there is little difference between the solid "blank" Macor piece and the sealed 4-layer package. However, both of these specimens had residual Helium levels that were significantly above the background level. This is disturbing and we investigated this phenomena.

Since the Macor is a composite material, we hypothesized that it might contain micro-crevices that could trap Helium beneath the surface. We imaged the solid Macor in the SEM to examine the size and character of the micro-crevices. Figure 4, below shows the surface of the Macor. Indeed the irregular topology and the crevices can be seen.

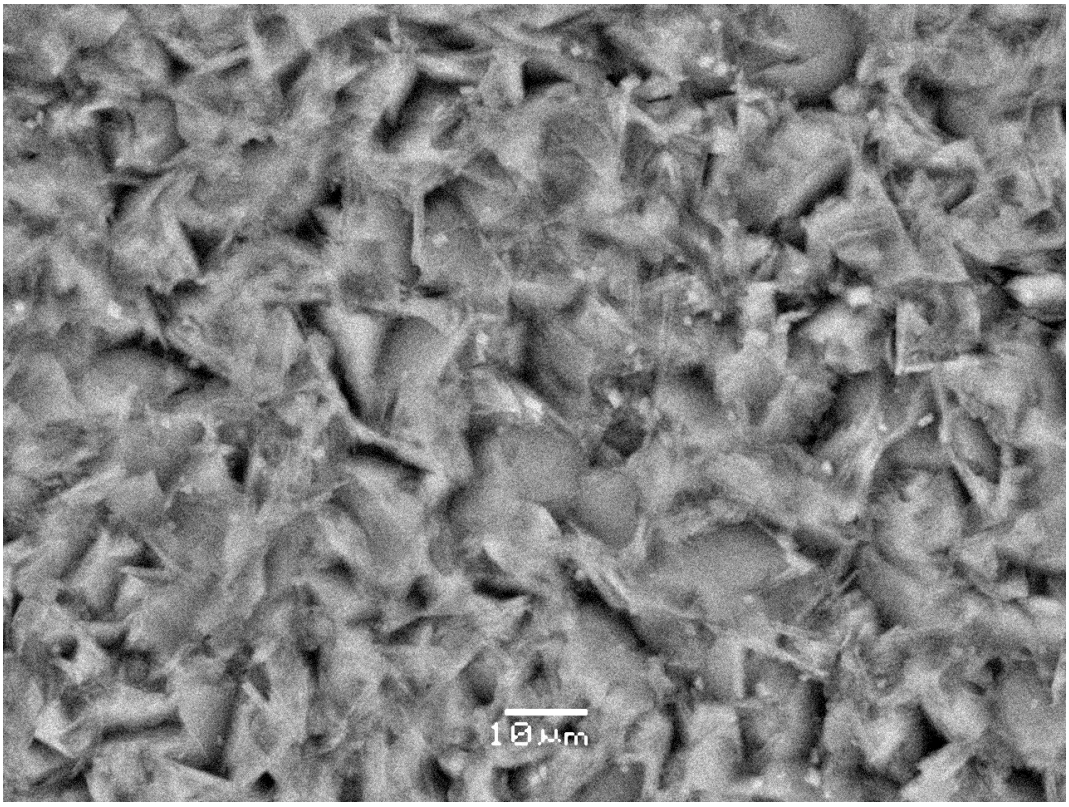


Figure 4 – SEM photograph of the surface of the Macor

However, the size of these crevices is well below the width of the glass seal. The glass seal is approximately 750 microns wide, whereas the average size of the crevices shown in Figure 4 is 10 microns. We then investigated whether the glass melts into the crevices at the interface between the glass and ceramic. Figures 5, 6, 7, and 8, show varying magnifications of the cross section between two ceramic sheets, and the glass seal.

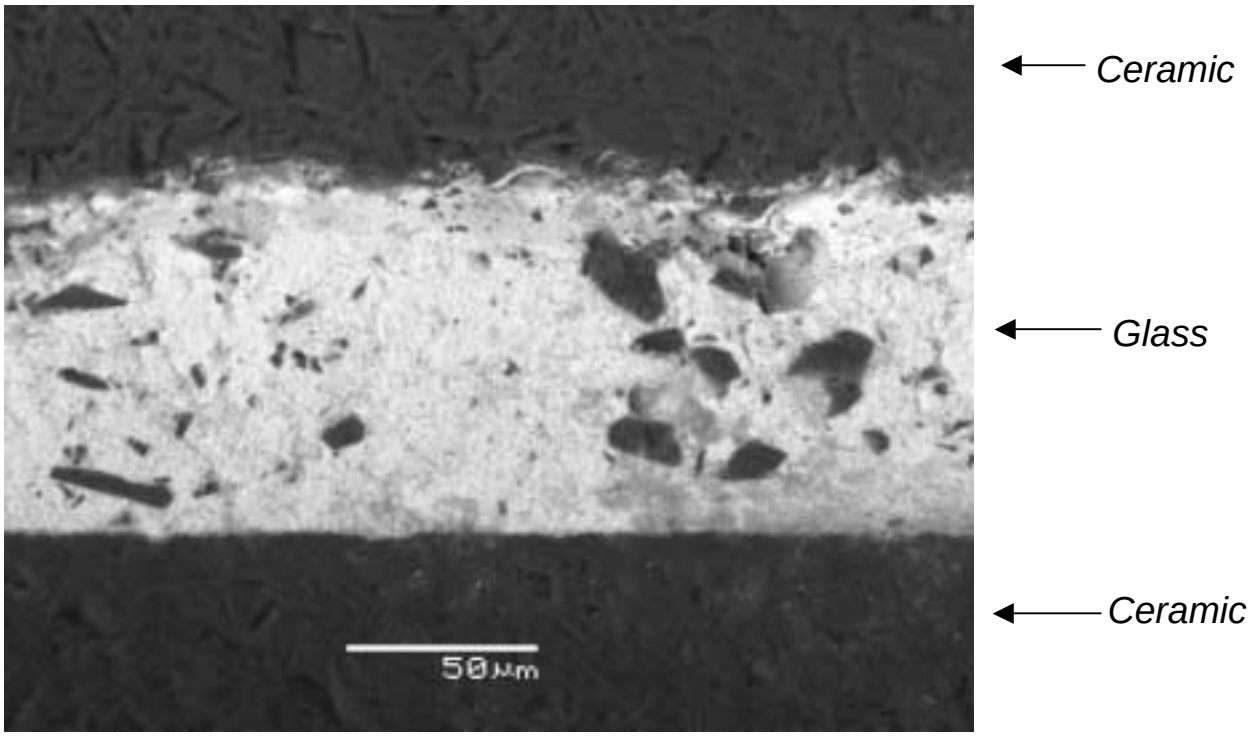
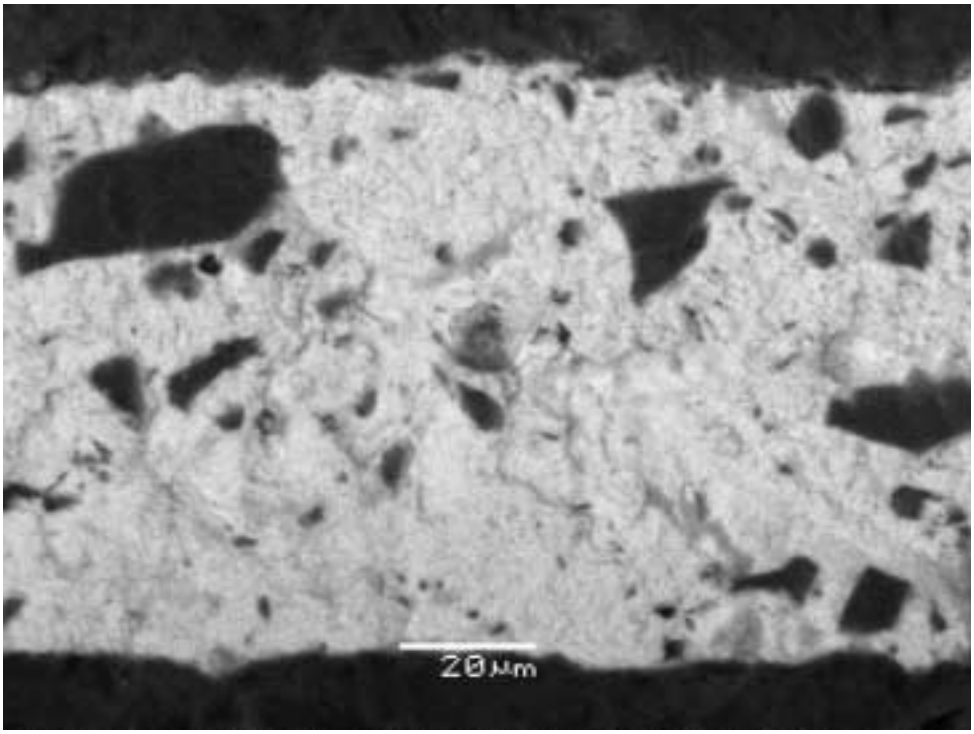


Figure 5 – Interface between two Macor sheets and the Glass seal (500x)



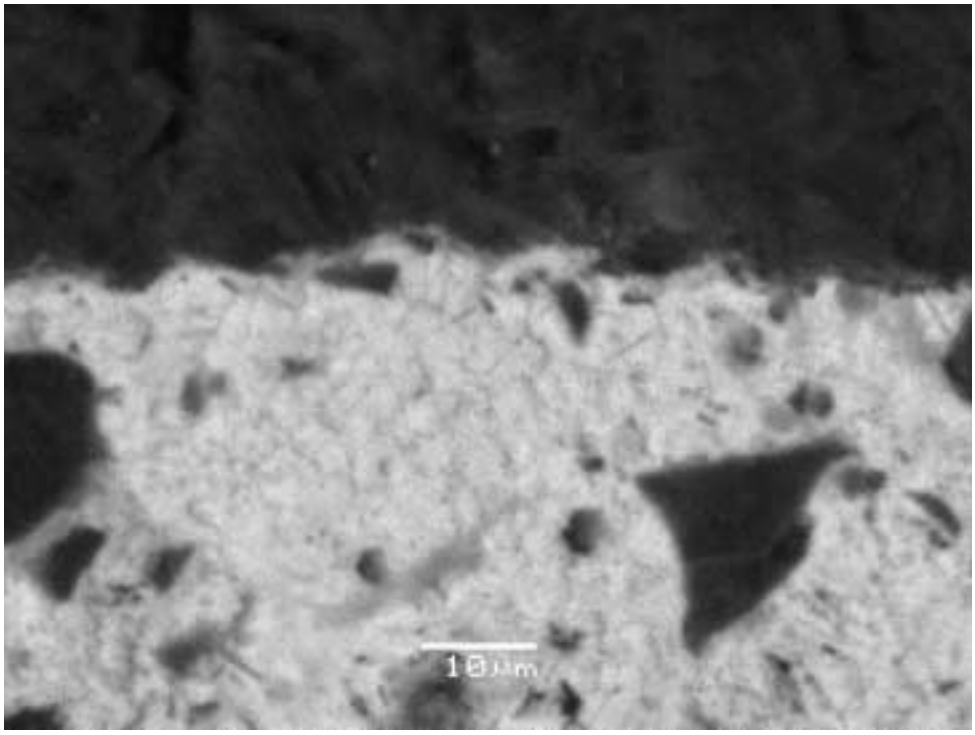
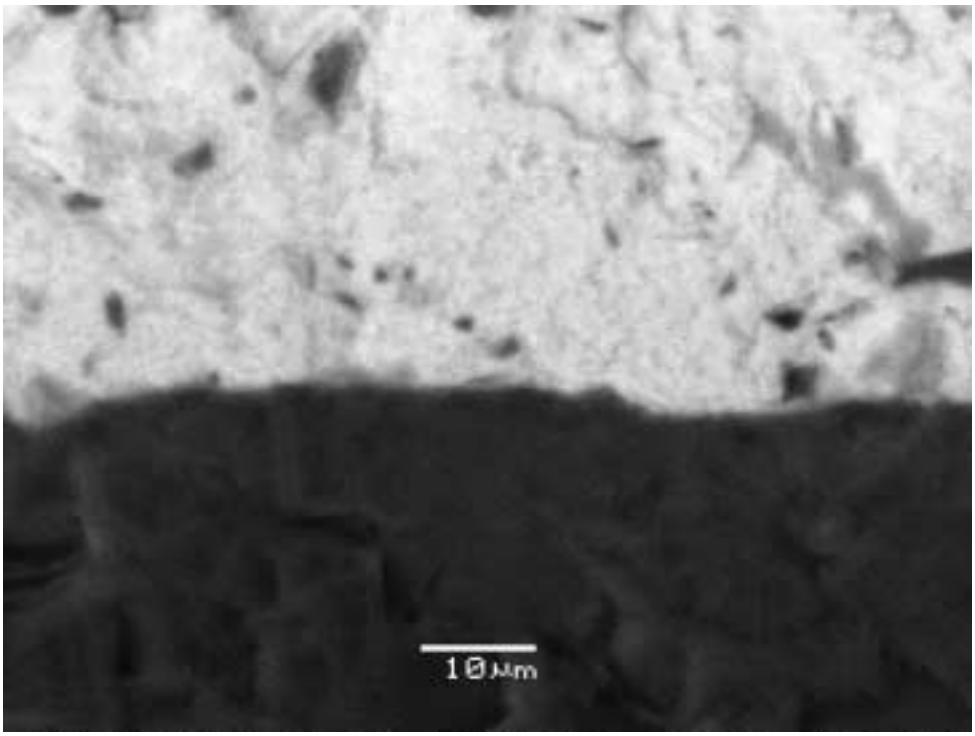


Figure 6 – Interface between two Macor sheets and the Glass seal (900x)

Figure 7 – Interface between upper Macor sheet and the Glass seal (1500x)
Figure 8 – Interface between lower Macor sheet and the Glass seal (1500x)



As can be seen in the SEM photos above, there is excellent integration between the glass and ceramic. This leads us to believe that the residual Helium seen in the Helium bomb test is an artifact of the measurement method and does not represent a leakage of the sealed package. We are researching, more thoroughly, the characteristics of Macor, through conversations with Corning Inc.

We are also preparing to do a direct measurement of water penetration into a sealed package by using impedance spectroscopy on traces buried within the cavity of the package. We are preparing special metallization patterns that will be electrically accessible by the package feedthroughs.

During the next quarter we intend to test the success of using extended-drain transistors in the output stage of the BLOCK chip in order to correct the small amount of residual imbalance between the anodic and cathodic phases, seen at high electrode voltages.